KPRIET

Learn Beyond

M.E. – VLSI Design

Curriculum and Syllabi

Regulations 2021

I. Vision and Mission of the Institute

Vision

To become a premier institute of academic excellence by imparting technical, intellectual and professional skills to students for meeting the diverse needs of the industry, society, the nation and the world at large.

Mission

- Commitment to offer value-based education and enhancement of practical skills
- Continuous assessment of teaching and learning process through scholarly activities
- Enriching research and innovative activities in collaboration with industry and institute of repute
- Ensuring the academic process to uphold culture, ethics and social responsibility

II. Vision and Mission of the Department

Vision

To be a department of repute for learning and research with state-of-the-art facilities to enable the students to succeed in globally competitive environment.

Mission

The Mission of the Department is to

- To impart knowledge and skill-based education with competent faculty striving for academic excellence.
- To instil research centres in the field, that industry needs, by collaborating with organizations of repute.
- To provide ethical and value-based education by promoting activities addressing the societal needs and facilitate lifelong learning.

III. Program Educational Objectives (PEOs)

PEO1: Analyze and solve complex VLSI circuits and systems through the acquired in-depth knowledge.

PEO2: Develop managerial skills and apply appropriate tools in the domains of VLSI design incorporating safety, sustainability and become a successful professional.

PEO3: Exhibit professionalism while communicating with local, national and foreign peers bound with regulations and leading life- long learning.

IV. Program Outcomes (POs)

At the end of the course, students will be able to

PO1: Apply the concepts of analog and digital circuits for IC design

PO2: Create, select and apply appropriate methods, systems and recent engineering and EDA tools including emulators for modeling and prototyping with an understanding of the tools limitations

PO3: Think laterally and originally to solve various problems in VLSI circuits and related domain after considering public health and safety, cultural, societal and environmental factors in the core areas of expertise

PO4: Independently carry out research /investigation and development work to solve practical problems

PO5: Write and present a substantial technical report/document

PO6: Demonstrate a degree of mastery in designing, developing and testing of VLSI circuits

V. PEO/PO Mapping

Following three levels of correlation should be used:

1: Low

2: Medium

3: High

	PO1	PO2	PO3	PO4	PO5	PO6
PEO1	3	2	1	2	2	3
PEO2	2	3	3	2	2	3
PEO3	1	2	3	2	3	2

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VI. MAPPING OF COURSE OUTCOMES WITH PROGRAM OUTCOMES

Year	SEM	Subject	PO1	PO2	PO3	PO4	PO5	PO6
I Year	SEM I	Analog Integrated Circuits Design	✓	✓	✓	-	-	✓
		Digital CMOS VLSI Design	✓	✓	✓	-	-	✓
		ASIC and FPGA Design	✓	✓	✓	-	-	✓
		Research Methodology and IPR	✓	✓	✓	✓	✓	✓
		Analog IC Design Laboratory	✓	✓	✓	✓	✓	✓
	SEM II	Low Power VLSI Design	✓	✓	✓	-	-	✓
		Testing of VLSI Circuits	✓	✓	✓	-	-	✓
		VLSI Signal Processing	✓	✓	✓	-	-	✓
		Digital IC Design Laboratory	✓	✓	✓	✓	✓	✓
II Year	SEM III	Project Work – Phase I						
	SEM IV	Project Work – Phase II						
PE		CAD for VLSI Circuits	✓	✓	✓	-	-	✓
		Advanced Nano Electronic Device Fabrication	✓	✓	✓	-	-	✓
		Advanced Digital System Design	✓	✓	✓	-	-	✓
		Design of System on Chip	✓	✓	✓	-	-	✓
		Scripting Language for VLSI	✓	✓	✓	-	-	✓
		System Verilog	✓	✓	✓	-	-	✓
		Design of Semiconductor memories	✓	✓	✓	-	-	✓

		Semiconductor Device Modeling	✓	✓	✓	-	-	✓
		Interconnections and Packaging for VLSI	✓	✓	✓	-	-	✓
		Hardware Verification Techniques	✓	✓	✓	-	-	✓
		IP based VLSI	✓	✓	✓	-	-	✓
		VLSI for Wireless Communication	✓	✓	✓	-	-	✓
		ARM Processor and Applications	✓	✓	✓	-	-	✓
		Industrial Internet of Things	✓	✓	✓	-	-	✓
		Security solutions in VLSI	✓	✓	✓	-	-	✓
		Thermal analysis and Power management of Integrated circuits	✓	✓	✓	-	-	✓
		Optimization Algorithm for VLSI	✓	✓	✓	-	-	✓
		MEMS and NEMS	✓	✓	✓	-	-	✓

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M.E. VLSI DESIGN

REGULATIONS – 2021

CHOICE BASED CREDIT SYSTEM

CURRICULUM FOR I TO IV SEMESTERS

SEMESTER I

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
THEORY							
1	P21VL101	Analog Integrated Circuits Design	PCC	3	0	0	3
2	P21VL102	Digital CMOS VLSI Design	PCC	3	0	0	3
3	P21VL103	ASIC and FPGA Design	FC	3	0	0	3
4	P21RMC01	Research Methodology and IPR	RMC	3	0	0	3
5		Professional Elective I	PEC	3	0	0	3
PRACTICALS							
6	P21VL104	Analog IC Design Laboratory	PCC	0	0	6	3
			TOTAL	**15**	**0**	**6**	**18**

SEMESTER II

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
THEORY							
1	P21VL201	Low Power VLSI Design	PCC	3	0	0	3
2	P21VL202	Testing of VLSI Circuits	PCC	3	0	0	3
3	P21VL203	VLSI Signal Processing	PCC	3	1	0	4
4		Professional Elective II	PEC	3	0	0	3
5		Professional Elective III	PEC	3	0	0	3
PRACTICALS							
6	P21VL204	Digital IC Design Laboratory	PCC	0	0	6	3
7	P21VL205	Technical Seminar	EEC	0	0	4	2
			TOTAL	**15**	**1**	**10**	**21**

SEMESTER III

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
THEORY							
1		Professional Elective IV	PEC	3	0	0	3
2		Professional Elective V	PEC	3	0	0	3
3		Professional Elective VI	PEC	3	0	0	3
PRACTICALS							
4	P21VL301	Project Work – Phase I	EEC	0	0	12	6
			TOTAL	**9**	**0**	**12**	**15**

SEMESTER IV

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
PRACTICALS							
1	P21VL401	Project Work – Phase II	EEC	0	0	24	12
			TOTAL	**0**	**0**	**24**	**12**

MANDATORY INTERNSHIP

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
1	P21VLI01	Industrial Training / Internship	EEC	0	0	4	2

***Four weeks during any semester vacation from I to IV semester**

Total Credit:68

LIST OF COURSES BASED ON ITS CATEGORY

FOUNDATION COURSES (FC)

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
1	P21VL103	ASIC and FPGA Design	FC	3	0	0	3

PROFESSIONAL CORE COURSES (PCC)

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
THEORY							
1	P21VL101	Analog Integrated Circuits Design	PCC	3	0	0	3
2	P21VL102	Digital CMOS VLSI Design	PCC	3	0	0	3
3	P21VL104	Analog IC Design Laboratory	PCC	3	0	0	3
4	P21VL201	Low Power VLSI Design	PCC	3	0	0	3

5	P21VL202	Testing of VLSI Circuits	PCC	3	0	0	3
6	P21VL203	VLSI Signal Processing	PCC	3	0	0	3
7	P21VL204	Digital IC Design Laboratory	PCC	3	0	0	3

PROFESSIONAL ELECTIVES COURSES (PEC)

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
1	P21VLP01	CAD for VLSI Circuits	PEC	3	0	0	3
2	P21VLP02	Advanced Nano Electronic Device Fabrication	PEC	3	0	0	3
3	P21VLP03	Advanced Digital System Design	PEC	3	0	0	3
4	P21VLP04	Design of System on Chip	PEC	3	0	0	3
5	P21VLP05	Scripting Language for VLSI	PEC	3	0	0	3
6	P21VLP06	System Verilog	PEC	3	0	0	3
7	P21VLP07	Design of Semiconductor memories	PEC	3	0	0	3
8	P21VLP08	Semiconductor Device Modeling	PEC	3	0	0	3
9	P21VLP09	Interconnections and Packaging for VLSI	PEC	3	0	0	3
10	P21VLP10	Hardware Verification Techniques	PEC	3	0	0	3
11	P21VLP11	IP based VLSI	PEC	3	0	0	3
12	P21VLP12	VLSI for Wireless Communication	PEC	3	0	0	3
13	P21VLP13	ARM Processor and Applications	PEC	3	0	0	3
14	P21VLP14	Industrial Internet of Things	PEC	3	0	0	3
15	P21VLP15	Security solutions in VLSI	PEC	3	0	0	3
16	P21VLP16	Thermal analysis and Power management of Integrated circuits	PEC	3	0	0	3
17	P21VLP17	Optimization Algorithm for VLSI	PEC	3	0	0	3
18	P21VLP18	MEMS and NEMS	PEC	3	0	0	3

RESEARCH METHODOLOGY & IPR COURSES (RMC)

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
1	P21RMC01	Research Methodology & IPR	RMC	3	0	0	3

EMPLOYABILITY ENHANCEMENT COURSES (EEC)

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
1	P21VL205	Technical Seminar	EEC	0	0	4	2

2	P21VL301	Project Work – Phase I	EEC	0	0	12	6
3	P21VL401	Project Work – Phase II	EEC	0	0	24	12
4	P21VLI01	Industrial Training / Internship	EEC	0	0	0	2

VIII. Scheme of Credit distribution – Summary

S.No	Stream	Credits/Semester				Credits	%	Suggested by AICTE
		I	II	III	IV			
1.	Foundation Courses (FC)	3	-	-	-	3	4.5%	3
2.	Professional Core Courses (PCC)	9	13	-	-	22	32%	20
3.	Professional Elective Courses (PEC)	3	6	9	-	18	26%	15
4.	Research Methodology & IPR Courses (RMC)	3	-	-	-	3	4.5%	3
5.	Employability Enhancement Courses (EEC)	-	2	6	12	20	30%	28
6.	Internship	-	-	-	-	2	3%	-
Total		**18**	**21**	**15**	**12**	**68**	**100**	**69**

SEMESTER I

P21VL101	ANALOG INTEGRATED CIRCUITS DESIGN	Category: PCC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Fundamentals of Electronic Circuits

COURSE OBJECTIVES:

- To study the basics of MOS devices and amplifiers
- To analyze the different performance parameters of operational amplifiers
- To learn the operations of bandgap references and switched capacitor circuits

UNIT I MOS DEVICE PHYSICS AND SINGLE STAGE AMPLIFIERS 9

MOS I/V characteristics – Second-Order effects – MOS device capacitances – MOS small-signal model – long channel versus short channel devices – Common Source stage with resistive load - Diode Connected load – Current Source load – Source follower

UNIT II DIFFERENTIAL AMPLIFIERS AND CURRENT MIRRORS 9

Single ended and differential operation – Common Mode response – Differential pair with MOS loads – Gilbert cell – Current sink and sources – Basic current mirrors – Cascade current mirrors – Active current mirrors – Large signal analysis and small signal analysis

UNIT III FREQUENCY RESPONSE OF AMPLIFIERS 9

Miller effect – Frequency response of Common Source Stage – Common Gate Stage and Source followers – Noise in single-stage amplifiers – Noise in differential pairs – Noise bandwidth – Effect of feedback on noise

UNIT IV OPERATIONAL AMPLIFIERS AND FREQUENCY COMPENSATION 9

Performance parameters – One-Stage Op amps – Two-Stage Op amps – Input Range Limitation – Power supply rejection – Multipole systems – Phase margin – Frequency compensation of two – stage Op Amps

UNIT V BANDGAP REFERENCES AND SWITCHED CAPACITOR CIRCUITS 9

Temperature independent references – PTAT current generation – Constant GM biasing – sampling switches – Switched capacitor amplifiers – Switched capacitor Common Mode feedback amplifiers – Switched capacitor integrator – Nonlinearity and mismatch

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", 2nd edition, McGraw Hill, 2017
2. Paul R.Gray, "Analysis and Design of Analog Integrated Circuits", 5th edition, John Wiley, 2009

REFERENCES:

1. Philip E.Allen, "CMOS Analog Circuit Design", 3rd edition, Oxford University Press, 2013
2. David A.Johns, Ken Martin, "Analog Integrated Circuit Design", 2nd edition, John Wiley & Sons, 2013
3. Jacob Baker, "CMOS Circuit Design Layout and Simulation", 3rd edition, Wiley IEEE Press, 2010

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Explain the fundamental concepts of MOS amplifiers	Understand
CO2	Inspect the performance of different current mirror circuits	Analyze
CO3	Examine the frequency response and noise effects in MOS amplifiers	Analyze
CO4	Illustrate the functionality of operational amplifiers	Understand
CO5	Summarize various switched capacitor amplifiers	Understand

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	3	3	3	-	-	2
CO3	3	3	3	-	-	2
CO4	2	1	1	-	-	-
CO5	2	1	1	-	-	-
CO	2	2	2	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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P21VL102	DIGITAL CMOS VLSI DESIGN	Category: PCC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Digital Electronics

COURSE OBJECTIVES:

- To learn the fabrication process and design methods of CMOS integrated circuit
- To study logic styles and sequential circuits of CMOS circuits
- To understand the VLSI subsystems and GaAs materials

UNIT I FABRICATION AND DESIGN PROCESS OF CMOS 9

MOS fabrication – nMOS, pMOS, BiCMOS – Stick diagram – Scaling – Design rules – Layout design of CMOS circuits – MOS transistor principles – Enhancement mode transistor operation – MOS DC equation

UNIT II LOGIC STYLES 9

Pass transistor and transmission gate – Static CMOS design – Pseudo NMOS – Dynamic CMOS logic – Clocked CMOS logic – Domino logic – Pre charged domino logic – Dual rail logic – CVSL – Keeper circuits

UNIT III SEQUENTIAL LOGIC 9

Conventional CMOS latches – CMOS D Flip Flop – SDFF – TSPC Flip Flop – CMOS static RAM – Dual port SRAM – SRAM arrays – DRAM and floating gate MOSFET – Flash memory

UNIT IV VLSI SUBSYSTEM DESIGN 9

CMOS based mux – Equality detector – Shift and rotation operation – Adders – Carry save, Carry select – Multipliers – Array, Braun, Wallace tree– 2's Complement, Baugh Wooley, Booth – Barrel shifter – ALU

UNIT V GALLIUM ARSENIDE MICROCIRCUITS 9

GaAs in VLSI – GaAs materials – Types of GaAs devices – Depletion mode transistor – Enhancement mode transistor – Enhancement/Depletion mode pairs – High electron mobility transistor – Self aligned transistor – Heterojunction bipolar transistor

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Jan M Rabaey, "Digital Integrated Circuits: A Design Perspective", 2nd edition, Prentice Hall, 2016
2. John P.Uyemura, "Introduction to VLSI circuits and systems", 2nd edition, John Wiley & Sons, 2006

REFERENCES:

1. Neil.H.E.Weste David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th edition, Pearson Addison Wesley, 2015
2. Kamran Eshraghian, Douglas A. Pucknell, "Essentials of VLSI Circuits and Systems", 3rd edition, Prentice Hall of India, 2015
3. E. Fabricious, "Introduction to VLSI Design", 1st edition, McGraw Hill, 2014
4. Sorab K. Ghandhi," VLSI Fabrication Principles", 2nd edition, John Wiley & Sons,2009

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Explain the fabrication and basics of CMOS transistor	Understand
CO2	Summarize the different logic styles of CMOS digital circuit	Understand
CO3	Make use of CMOS logic to design sequential circuits	Apply
CO4	Categorize the VLSI sub systems based on design parameters	Analyze
CO5	Illustrate the fundamentals of microcircuits using GaAs	Understand

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	3	2	3	-	-	1
CO4	3	3	3	-	-	2
CO5	2	1	1	-	-	-
CO	2	2	2	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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P21VL103	ASIC AND FPGA DESIGN	Category: FC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Digital Electronics

COURSE OBJECTIVES:

- To study the fundamentals of ASIC
- To understand the different FPGA architectures
- To learn low level design languages

UNIT I BASICS OF ASIC 9

Types of ASICs – Design Flow – Economics of ASICs – ASIC Cell Library – Library Cell Design – Library Architecture – Gate Array Design – Datapath Cell Design

UNIT II PROGRAMMABLE ASIC 9

Antifuse – Metal-Metal Antifuse – FPGAs in Use – Specifications – PREP Benchmarks – FPGA Economics – FPGA Pricing – Pricing Examples – Actel ACT 205 – Xilinx LCA 218 – Altera FLEX 223 – Altera MAX 223

UNIT III PROGRAMMABLE ASIC I/O CELLS 9

DC Output 246 – AC Output 249 – DC Input 257 – AC Input 262 – Clock Input 267 – Power Input 269 – Xilinx I/O Block 272

UNIT IV PROGRAMMABLE ASIC INTERCONNECT 9

Actel ACT 289 – Xilinx LCA 298 – Xilinx EPLD 302 – Altera MAX 5000 and 7000 303 – Altera MAX 9000 304 – Altera Flex 305 – Design Systems – FPGA Logic Synthesis – Halfgate ASIC 321

UNIT V LOW LEVEL DESIGN ENTRY 9

Schematic Entry – Hierarchical Design – Schematic Icons and Symbols – Nets – Vectored Instances and Buses – Netlist Screener – Low Level Design Languages – PLA Tools – CFI Design Representation

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. M.J.S.Smith, "Application Specific Integrated Circuits", 2nd edition ,Pearson Education, 2010
2. Ming-Bo Lin, "Digital System Designs and Practices using Verilog HDL and FPGAs", 7th edition Wiley, 2012

REFERENCES:

1. Samir Palnitkar, "Verilog HDL", 2nd edition Pearson Education, 2004
2. J.Bhaskar, "A VHDL Primer", 3rd edition ,Prentice Hall- 1998
3. J.Bhaskar, "A Verilog Primer",5th edition, Prentice Hall- 2005
4. Bob Zeidman, "Designing with FPGAs and CPLDs", 4th edition, Elsevier, CMP Books, 2002

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Explain the fundamental Concepts of ASIC	Understand
CO2	Summarize the design specifications of FPGA	Understand
CO3	Infer the inputs and outputs of programming in ASIC	Understand
CO4	Illustrate the different FPGA architecture and logic synthesis	Understand
CO5	Compare the performance of different low level design languages	Analyze

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	2	1	1	-	-	-
CO4	2	1	1	-	-	-
CO5	3	3	3	-	-	2
CO	2	1	1	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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P21RMC01	RESEARCH METHODOLOGY AND IPR	Category: RMC			
		L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To impart knowledge in problem formulation, analysis and solutions.
- To impart skills required for technical paper writing / presentation without violating professional ethics
- To familiarize knowledge on Patent drafting and filing patents

UNIT I RESEARCH PROBLEM FORMULATION 9

Meaning of research problem – Sources of research problem – Criteria characteristics of a good research problem – Errors in selecting a research problem – Scope and objectives of research problem. Approaches of investigation of solutions for research problem – data collection – analysis – interpretation – necessary instrumentations

UNIT II LITERATURE REVIEW AND DATA COLLECTION 9

Effective literature studies approaches – analysis – plagiarism and research ethics. Method of data collection, Types of data – Primary Data – Scales of measurement – Source and collection of data observation method – Secondary data

UNIT III TECHNICAL WRITING / PRESENTATION 9

Effective technical writing: How to write report – paper – developing a research proposal – format of research proposal – a presentation and assessment by a review committee

UNIT IV INTRODUCTION TO INTELLECTUAL PROPERTY RIGHTS (IPR) 9

Nature of Intellectual Property: Patents – Designs – Trade and Copyright. Process of Patenting and Development – technological research – innovation, patenting – development – International Scenario – International cooperation on Intellectual Property – Procedure for grants of patents – Patenting under PCT

UNIT V INTELLECTUAL PROPERTY RIGHTS (IPR) 9

Patent Rights: Scope of Patent Rights – Licensing and transfer of technology – Patent information and databases – Geographical Indications – New Developments in IPR – Administration of Patent System – IPR of Biological Systems – Computer Software etc.,

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: –Periods Total: 45 Periods

REFERENCES:

1. Ranjit Kumar, "Research Methodology: A Step-by-Step Guidefor beginners" 2nd Edition, 2014
2. Cooper, DR and Schindler, P S., "Business Research Methods", Tata McGraw Hill, 9th Edition, 2018
3. Robert P. Merges, Peter S, Menell, Mark A. Lemley, "Intellectual Property" in New Technological age, 2020

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Formulate research problem	Apply
CO2	Carry out research analysis	Analyse
CO3	Develop research proposal	Evaluate
CO4	Draft process of patenting	Apply
CO5	File and publish patents in R & D.	Evaluate

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	3	-	-	1
CO2	3	3	3	-	-	2
CO3	3	3	3	-	-	2
CO4	3	2	3	-	-	1
CO5	3	3	3	-	-	2
CO	3	3	3	-	-	2

Correlation levels: 1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High)

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P21VL104	ANALOG IC DESIGN LABORATORY	Category: PCC			
		L	T	P	C
		0	0	6	3

PRE–REQUISITES:

- Analog electronics

COURSE OBJECTIVES:

- To learn cadence tool
- To study the fundamental principles of CMOS circuits
- To understand the design of analog circuits using cadence

SUGGESTED LIST OF EXPERIMENTS

I. Pre-layout and post layout simulation using Cadence

1. Characterization of NMOS and PMOS Transistor
2. Design of Common Source Amplifier with different Loads
3. Design of Common Gate Amplifier
4. Design of Common Drain Amplifier
5. Design of Single stage Cascode Amplifiers
6. Design of Current Mirrors
7. Design of Differential Amplifiers with Different Loads
8. Design of Two stage Opamp
9. Design of Telescopic Cascode Opamp
10. Design of Folded Cascode Opamp
11. Design of 6T-SRAM
12. Transient analysis of RC delay model
13. Analysis of frequency response of current series and current shunt feedback topologies.
14. Analysis of frequency response of voltage series and voltage shunt feedback topologies.
15. Analysis of Circuits - Power Planning, Layout generation, LVS and Back annotation, Total power estimation

Contact Periods:

Lecture: – Periods Tutorial: – Periods Practical: 90 Periods Total: 90 Periods

COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Make use of Cadence tool for MOS transistor characterization.	Apply
CO2	Build various types of analog amplifiers for the given specifications.	Apply
CO3	Construct Wilson and Widlar current mirror circuits.	Apply
CO4	Examine the performance of different types of OPAMP	Analyze
CO5	Analyze the frequency response of feedback amplifiers	Analyze

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COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	3	2	3	1
CO2	3	2	3	2	3	1
CO3	3	2	3	2	3	1
CO4	3	3	3	2	3	2
CO5	3	3	3	2	3	2
CO	3	2	3	2	3	1
Correlation levels: (High)	1: Slight (Low)		2: Moderate (Medium)		3: Substantial	

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SEMESTER II

P21VL201	LOW POWER VLSI DESIGN	Category: PCC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- VLSI Design

COURSE OBJECTIVES:

- To learn different sources of power dissipation and power estimation in CMOS
- To study the concept for synthesis of different level low power transforms
- To understand low power static RAM architecture & energy recovery techniques used in low power design

UNIT I POWER DISSIPATION IN CMOS 9

Sources of power dissipation – Physics of power dissipation in MOSFET devices: The MIS structure, long channel MOSFET, submicron MOSFET and gate induced drain leakage – Power dissipation in CMOS: short circuit dissipation, dynamic dissipation and load capacitance

UNIT II POWER ESTIMATION 9

Modelling of signals – Signal probability calculation – Statistical techniques – Estimation of glitching power sensitivity analysis – Power estimation using input vector compaction, power dissipation in domino logic, circuit reliability, power estimation at the circuit level

UNIT III SYNTHESIS FOR LOW POWER 9

Behavioral level transforms – Software design algorithms – Parallel implementation – Pipelined implementation – Logic level optimization – Technology dependent and independent circuits

UNIT IV LOW POWER STATIC RAM ARCHITECTURES 9

Organization of a static RAM– MOS static RAM memory cell– Banked organization of SRAMs – Reducing voltage swings on bit lines – Reducing power in the write diver circuits – Reducing power in sense amplifier circuits

UNIT V LOW ENERGY COMPUTING USING ENERGY RECOVERY TECHNIQUES 9

Energy dissipation in transistor channel using an RC model – Energy recovery circuit design – Designs with partially reversible logic – Supply clock generation

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. K.Roy and S.C. Prasad, "Low Power CMOS VLSI Circuit Design", 3rd edition, Wiley, 2014
2. K.S. Yeo and K.Roy, "Low Voltage Low Power VLSI Subsystems", 2nd edition, Tata McGrawHill, 2016

REFERENCES:

1. Dimitrios Soudris, Chirstian Pignet and Costas Goutis, "Designing CMOS Circuits for Low Power", 1st edition, Kluwer, 2009
2. James B. Kuo and Shin Chia Lin, "Low voltage SOI CMOS VLSI Devices and Circuits", 2nd edition, John a Wiley and Sons, 2012
3. J.B Kuo and J.H Lou,"Low voltage CMOS VLSI Circuits", 2nd edition, Wiley, 2009
4. Gary Yeap, "Practical Low Power Digital VLSI Design", 4th edition, Kluwer, 2012

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Interpret the concept of power dissipation in CMOS	Understand
CO2	Illustrate the different power estimation techniques	Understand
CO3	Apply the Behavioral level transforms for logical level optimization	Apply
CO4	Explain the static RAM architecture for reducing power in the circuits	Understand
CO5	Examine the low energy computation using appropriate energy recovery techniques	Analyze

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	3	2	3	-	-	1
CO4	2	1	1	-	-	-
CO5	3	3	3	-	-	2
CO	2	2	2	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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P21VL202	TESTING OF VLSI CIRCUITS	Category: PCC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Digital design

COURSE OBJECTIVES:

- To understand basics of simulation techniques and test generation
- To learn different types of test methods for combinational and sequential circuits
- To study the concepts behind different types of test for fault identification

UNIT I FAULT SIMULATION 9

Introduction to testing – Faults in digital circuits – Modeling of faults – Logical fault models – Fault detection – Fault location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate level event–driven simulation

UNIT II TEST GENERATION 9

Test generation for combinational logic circuits – Testable combinational logic circuit design –Test generation for sequential circuits – Design of testable sequential circuits – Ad hoc design and scan–based design techniques

UNIT III ANALOG AND MIXED SIGNAL TEST 9

DSP based analog and mixed signal test – Static ADC and DAC testing methods – Model based Analog and mixed signal test – Analog fault models – Analog fault simulation – Analog ATPG

UNIT IV BUILT IN SELF–TEST 9

Built–In self–test – Test pattern generation for BIST – Circular BIST – BIST architecture – Testable memory design – Test algorithms – Test generation for embedded RAMs

UNIT V DESIGN FOR TESTABILITY 9

Adhoc design for testability techniques – Controllability and observability by means of scan registers – Storage cells for scan designs – Level sensitive scan design (LSSD) – Partial scan – Boundary scan

Contact Periods:

Lecture: 45 Periods Tutorial: –Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Abramovici .M, Breuer M.A and Friedman A.D, "Digital Systems and Testable Design", 2nd edition, Jaico Publishing House, 2002
2. Bushnell M.L and Agrawal V.D, "Essentials of Electronic Testing for Digital Memory and Mixed–Signal VLSI Circuits", 1st edition, Kluwer Academic Publishers, 2004

REFERENCES:

1. Lala P.K, "Digital Circuit Testing and Testability",1st edition, Academic Press, 1997
2. Parag K. Lala, "Self–checking and fault tolerant digital design", 1st edition, Morgan Kaufmann, 2006
3. Xiaoqing Wen, Cheng Wen Wu and Laung Terng Wang, "VLSI Test Principles and Architectures: Design for Testability", 1st edition, Cambridge University Press, 2006
4. Stanely L Hurst,"VLSI Testing: Digital and mixed analogue digital techniques", 1st edition, Institute of Electrical Engineering, 1998

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Explain fundamentals of fault simulation	Understand
CO2	Compare test generation for combinational and sequential circuits	Understand
CO3	Choose the appropriate testing methods for fault simulation	Apply
CO4	Illustrate various BIST architecture and different test algorithms	Understand
CO5	Test for fault identification using DFT approach	Analyze

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	3	2	3	-	-	1
CO4	2	1	1	-	-	-
CO5	3	3	3	-	-	2
CO	2	2	2	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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P21VL203	VLSI SIGNAL PROCESSING	Category: PCC			
		L	T	P	C
		3	1	0	4

PRE–REQUISITES:

- Digital Signal Processing

COURSE OBJECTIVES:

- To learn various methods for critical path reduction
- To design digital filters and arithmetic architectures
- To understand pipelining concepts in digital filters

UNIT I METHODS OF CRITICAL PATH REDUCTION 9

Introduction to digital signal processing systems - Iteration bound – Pipelining and parallel processing – Retiming – Unfolding – Systolic architecture design

UNIT II ALGORITHMIC STRENGTH REDUCTION METHODS 9

Fast convolution – Parallel FIR filters – Discrete Cosine Transform and inverse DCT – Parallel architecture for rank order filters – Pipelined and parallel recursive and adaptive filters.

UNIT III DESIGN OF DIGITAL FILTERS 9

Scaling and round off noise – Schur algorithm – Digital basic lattice filters – One multiplier lattice filter – Normalized lattice filter – Pipelining of lattice IIR digital filters.

UNIT IV DESIGN OF ARITHMETIC ARCHITECTURES 9

Bit level arithmetic architectures – Redundant number representations – Radix -2 and Radix – 4 addition and subtraction – Data format conversion – Redundant to non-redundant converter

UNIT V PIPELINING CONCEPTS 9

Synchronous pipelining and clock styles – Clock skew and clock distribution – Wave pipelining – Constraint space diagram and degree of wave pipelining – Asynchronous pipelining

Contact Periods:

Lecture: 45 Periods Tutorial: NIL Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Keshab K.Parhi, "VLSI Digital Signal Processing Systems, Design and Implementation", John Wiley, Indian Reprint, 2007
2. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Arrays", Springer, 2nd edition, Indian Reprint, 2014

REFERENCES:

1. J. G. Chung and Keshab K. Parhi, "Pipelined Lattice and Wave Digital Recursive Filters", Springer Publisher, 1996
2. Mohammed Isamail and Terri Fiez, "Analog VLSI Signal and Information Processing", McGraw-Hill, 1994
3. S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985
4. Jose E. France, Yannis Tsividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Summarize various critical path reduction techniques	Understand
CO2	Construct pipelined and parallel FIR filters	Apply
CO3	Simplify the design of lattice filters	Analyse
CO4	Outline bit level and redundant arithmetic architectures	Understand
CO5	Illustrate various synchronous and asynchronous pipelining concepts	Understand

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	3	2	3	-	-	1
CO3	3	3	3	-	-	2
CO4	2	1	1	-	-	-
CO5	2	1	1	-	-	-
CO	2	2	2	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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P21VL204	DIGITAL IC DESIGN LABORATORY	Category: PCC			
		L	T	P	C
		0	0	6	3

PRE–REQUISITES:

- Fundamentals of digital logic design

COURSE OBJECTIVES:

- To design digital IC circuits.
- To implement pipeline based FIR algorithm.
- To apply fault detection methods to various digital circuits.

LIST OF EXPERIMENTS

I. Simulation and Implementation in FPGA

1. Design of 8-bit Carry Skip Adder and Carry Save Adder
2. Design of 4-bit Array Multiplier with and without Pipelining
3. Design of 4-tap FIR Filter with and without Pipelining
4. Design of FIFO
5. Design of Sequence Detector
6. Design of 8-bit ALU
7. Design and implementation of seven segment display

II. Prelayout and post layout simulation using Cadence

8. Comparator
9. Shift Register and Universal Shift Register
10. Synchronous up counter and down counter
11. Design of FFT
12. Memory – ROM, RAM

III. Testing of VLSI circuits

1. Design and simulation of BIST architecture for SRAM
2. Fault detection and diagnosis for combinational circuits
3. Fault detection and diagnosis for sequential circuits

Contact Periods:

Lecture: – Periods Tutorial: – Periods Practical: 90 Periods Total: 90 Periods

COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Develop HDL code for combinational circuits.	Apply
CO2	Build HDL code for sequential circuits.	Apply
CO3	Examine the Fault detection and diagnosis.	Analyze
CO4	Make use of FPGA kit for Implementation for hardware modules.	Apply
CO5	Utilize the different backend tools for digital circuits.	Apply

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COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	3	2	3	1
CO2	3	2	3	2	3	1
CO3	3	3	3	2	3	2
CO4	3	2	3	2	3	1
CO5	3	2	3	2	3	1
CO	3	2	3	2	3	1
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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ELECTIVE I

P21VLP01	CAD FOR VLSI CIRCUITS	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- VLSI Design principles

COURSE OBJECTIVES:

- To understand VLSI design flow and methodologies
- To learn floor planning and routing
- To study simulation and high-level synthesis

UNIT I VLSI DESIGN FLOW 9

Introduction to VLSI design flow and design methodologies – Evolution of CAD tools – Classification of CAD tools – Overview of VLSI design automation tools and algorithms – Tractable and Intractable problems – General purpose methods for combinatorial optimization

UNIT II PARTITIONING AND PLACEMENT 9

Layout compaction – Design rules- Problem formulation – Algorithms for constraint graph compaction – Placement and Partitioning – Circuit representation – Placement algorithms – Partitioning

UNIT III FLOOR PLANNING AND ROUTING 9

Floor planning concepts – Shape functions and floor plan sizing – Types of local routing problems – Area routing – Channel routing – Global routing – Algorithms

UNIT IV SIMULATION AND LOGIC SYNTHESIS 9

Simulation – Gate level modeling and simulation – Switch-level modeling and simulation – Combinational Logic Synthesis – Binary Decision Diagrams (BDD)

UNIT V MODELLING AND HIGH LEVEL SYNTHESIS 9

High level synthesis – Hardware models – Internal representation – Allocation – Assignment and scheduling – Simple scheduling algorithm – Assignment problem

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Gerez, S.H., "Algorithms for VLSI Design Automation",2nd edition, John Wiley & Sons, 2006
2. Sherwani, N.A., "Algorithms for VLSI Physical Design Automation", 3rd edition Kluwer Academic Publishers, 2002

REFERENCES:

1. Sadiq M. Sait, Habib Youssef, "VLSI Physical Design automation: Theory and Practice", 2nd edition, World Scientific, 1999
2. Drechsler, R., "Evolutionary Algorithms for VLSI CAD", 5th edition, Kluwer Academic Publishers, 1998
3. Stephen Trimberger, "Introduction to CAD for VLSI", 2nd edition, Kluwer Academic publisher, 2002

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Explain VLSI design automation tools	Understand
CO2	Choose appropriate algorithm for partitioning and placement	Apply
CO3	Identify suitable algorithms for placement and floor planning	Apply
CO4	Examine the optimized gate level representation of combinational circuits	Analyze
CO5	Summarize hardware model for high level synthesis	Understand

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	3	2	3	-	-	1
CO3	3	2	3	-	-	1
CO4	3	3	3	-	-	2
CO5	2	1	1	-	-	-
CO	3	2	2	-	-	1
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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P21VLP02	ADVANCED NANO ELECTRONIC DEVICE FABRICATION	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Basic understanding of semiconductor devices.

COURSE OBJECTIVES:

- To learn about fundamentals of classical CMOS technology and understand the issues in scaling MOSFET in the sub-100nm regime.
- To understand the need of non classical device structures and novel materials to reduce short channel effects.
- To study extensive characterization techniques used for high performance transistors.

UNIT I INTRODUCTION TO NANOELECTRONICS 8

Overview: Nano devices, Nano materials, Nano characterization - Definition of Technology node, Basic CMOS Process flow - MOS Scaling theory, Issues in scaling MOS transistors: Short channel effects, Description of a typical 65 nm CMOS technology - Requirements for Non classical MOS transistor.

UNIT II MOS ELECTRICAL CHARACTERIZATION AND TRANSISTOR DESIGN TECHNIQUES 8

MOS capacitor, Role of interface quality and related process techniques, Gate oxide thickness scaling trend, SiO2 vs High-k gate dielectrics. Integration issues of high-k . Interface states, bulk charge, band offset, stability, reliability – Qbd high field, possible candidates, CV and IV techniques - Metal gate transistor: Motivation, requirements, Integration Issues

UNIT III NON CLASSICAL MOSFETS 8

Transport in Nano MOSFET, velocity saturation, ballistic transport, injection velocity, velocity overshoot - SOI - PDSOI and FDSOI - Ultrathin body SOI – double gate transistors, integration issues - Vertical transistors: FinFET and Surround gate FET - Metal source/drain junctions: Properties of schotky junctions on Silicon, Germanium and compound semiconductors: Workfunction pinning.

UNIT IV INTRODUCTION TO NANO MATERIALS AND FABRICATION PROCESS 10

Germanium Nano MOSFETs: strain, quantization, Advantages of Germanium over Silicon, PMOS versus NMOS. Compound semiconductors – material properties, MESFETs Compound semiconductors MOSFETs in the context of channel quantization and strain, Heterostructure MOSFETs exploiting novel materials, strain, quantization - Synthesis of Nanomaterials: CVD, Nucleation and Growth, ALD, Epitaxy, MBE

UNIT V CHARACTERIZATION OF NANO MATERIALS AND NANO STRUCTURES 11

Compound semiconductor hetero-structure growth and characterization: Quantum wells - Thickness measurement techniques: Contact - step height, Optical - reflectance and ellipsometry. AFM – Characterization techniques for nanomaterials: FTIR, XRD, AFM, SEM, TEM, EDAX etc. Applications and interpretation of results. Emerging nano materials: Nanotubes, nanorods and other nano structures, LB technique, Soft lithography etc. Microwave assisted synthesis, Self assembly etc.

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Fundamentals of Modern VLSI Devices, Y. Taur and T. Ning, Cambridge University Press, 2006.
2. Silicon VLSI Technology, Plummer, Deal, Griffin, Pearson Education India, 2008.
3. Encyclopedia of Materials Characterization, Edited by: Brundle, C.Richard; Evans, Charles A. Jr.; Wilson, Shaun; Elsevier, 2003

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Illustrate the fundamentals of classical CMOS technology and the issue in scaling MOSFET in the sub-100nm regime	Understand
CO2	Explain need for non classical transistors with new device structure and nano materials	Understand
CO3	Examine the issues in realizing Germanium and compound semiconductor MOSFET	Analyze
CO4	Summarize extensive materials characterization techniques	Understand
CO5	Present the state of the art in the areas of semiconductor device physics and materials technology to enable the Nanoelectronics.	Apply

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	3	3	3	-	-	2
CO4	2	1	1	-	-	-
CO5	3	2	3	-	-	1
CO	2	2	2	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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P21VLP03	ADVANCED DIGITAL SYSTEM DESIGN	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Digital Electronics, VLSI

COURSE OBJECTIVES:

- To design synchronous and asynchronous sequential network using different techniques
- To learn the basics of programmable logic devices and state machine design
- To study fault tolerance diagnosis and fault tolerant methods

UNIT I SYNCHRONOUS SEQUENTIAL NETWORKS 9

Analysis of clocked synchronous sequential networks – Modeling of clocked synchronous sequential networks – State stable assignment – State table reduction – Design of clocked synchronous sequential networks – Algorithmic state machine charts

UNIT II ASYNCHRONOUS SEQUENTIAL NETWORKS 9

Analysis of Asynchronous Sequential Circuits (ASC) – Flow table reduction – Races in ASC – State assignment – Problems and the transition table – Design of ASC – Static and dynamic hazards – Essential hazards

UNIT III PROGRAMMABLE LOGIC DEVICES 9

Introduction to PLD – Types of PLD – ROM – Organization and combinational logic design using ROM – Programmable logic arrays – Design – Programmable array logic – PLD based state machine design

UNIT IV FAULT DIAGNOSIS AND TEST GENERATION METHODS 9

Modeling of faults in digital circuits – Temporary faults – Fault diagnosis – Test generation for combinational logic circuits – Path sensation – Boolean difference – D algorithm – PODEM – Detection of multiple faults – Test generation for sequential circuits – Random testing

UNIT V FAULT TOLERANT AND DESIGN FOR TESTABILITY 9

Introduction of fault tolerance – Dynamic redundancy – Hybrid redundancy – Fault tolerant design of memory systems using error correcting codes – Controllability and absorbability – Built in self test

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Donald D Givone, "Digital principles and Design", 3rd edition, Tata McGraw Hill,2015
2. Comer, "Digital Logic and State Machine Design", 3rd edition, Oxford University Press, 2014

REFERENCES:

1. Parag K Lala, "Fault Tolerant and Fault Testable Hardware Design", 2nd edition, BS publication, 2009
2. John Yarbrough M, "Digital Logic applications and Design", 2nd edition, Thomson Learning, 2006
3. Stephen Brown and Zvonk Vranesic, "Fundamentals of Digital Logic with VHDL Design", 3rd edition, Tata McGraw Hill, 2008
4. Charles Roth Jr .H, "Digital System Design using VHDL", 2nd edition, Thomson Learning, 2007

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Analyze synchronous sequential networks for digital circuits	Analyze
CO2	Examine the performance of asynchronous sequential networks.	Analyze
CO3	Make use of programmable logic devices to design combinational logic circuits	Apply
CO4	Summarize different test generation methods for fault diagnosis	Understand
CO5	Explain fault tolerance design of memory systems	Understand

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	-	-	2
CO2	3	3	3	-	-	2
CO3	3	2	3	-	-	1
CO4	2	1	1	-	-	-
CO5	2	1	1	-	-	-
CO	3	2	2	-	-	2

Correlation levels: 1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High)

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ELECTIVE II

P21VLP04	DESIGN OF SYSTEM ON CHIP	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- VLSI design

COURSE OBJECTIVES:

- To learn the fundamental of concepts system design
- To study the different processors and memories of SoC
- To understand about interconnect architectures and testing in design

UNIT I FUNDAMENTALS TO THE SYSTEM APPROACH 9

System architecture - Components of the system - Hardware and software- Processor architectures - Memory and addressing - System level interconnection - An approach for SOC design - System architecture and complexity

UNIT II SYSTEM-LEVEL DESIGN 9

Processor Selection for SOC - Concepts in processor architecture and processor micro architecture - Elements in instruction handling – Buffers - Minimizing pipeline delays - Branches - More robust processors - Vector processors and vector instructions extensions - VLIW Processors - Superscalar processors.

UNIT III MEMORY DESIGN FOR SoC 9

SOC external memory - Internal memory – Size - Scratchpads and cache memory - Cache Organization - Cache data - Write policies - Strategies for line replacement at miss time - Types of cache - Split I and D caches - Multilevel caches - Virtual to real translation - SOC memory system - Models of simple processor – Memory interaction.

UNIT IV INTERCONNECT CUSTOMIZATION AND CONFIGURATION 9

Interconnect architectures - Bus - Basic architectures - SOC standard buses - Analytic bus models - Using the bus model - Effects of bus transactions and contention time - SOC customization - Customizing instruction processor - Reconfiguration technologies - Mapping design onto reconfigurable devices - Instance specific design - Customizable soft processor

UNIT V SoC IMPLEMENTATION AND TESTING 9

Processor IP - Memory IP - Wrapper design - Real-time operating system (RTOS) - Peripheral interface and components – High density FPGAs - EDA tools used for SoC design - Manufacturing test of SoC - Core layer - System layer - Application layer - P1500 Wrapper standardization - SoC Test Automation (STAT).

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip", 1st edition Wiley India Pvt. Ltd, 2011
2. Sudeep Pasricha, Nikil Dutt, "On Chip Communication Architectures: System on Chip Interconnect", 2nd edition, Morgan Kaufmann Publishers, 2008

REFERENCES:

1. Steve Furber, "ARM System on Chip Architecture ", 2nd edition, Addison Wesley Professional, 2000
2. Ricardo Reis, "Design of System on a Chip: Devices and Components", 1st edition, Springer, 2004

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3. Prakash Rashinkar, Peter Paterson and Leena Singh L, "System on Chip Verification – Methodologies and Techniques", 2nd edition, Kluwer Academic Publishers,2001
4. C.Rowen," Engineering the Complex SOC: Fast, Flexible Design with Configurable Processors, 1st edition, Prentice Hall, 2004.

COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Outline the fundamentals of system on chip	Understand
CO2	Summarize different processors used in system design	Understand
CO3	Illustrate the different approaches of SoC memory design	Understand
CO4	Identify the appropriate architecture for interconnect customization	Apply
CO5	Analyze the performance of EDA tools in design and testing	Analyze

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	2	1	1	-	-	-
CO4	3	2	3	-	-	1
CO5	3	3	3	-	-	2
CO	2	2	2	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)			3: Substantial (High)

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P19VLP05	SCRIPTING LANGUAGE FOR VLSI	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Programming Language

COURSE OBJECTIVES:

- To study requirements of software systems for implementing the scripting languages
- To apply PERL scripting for simple applications.
- To understand multi-paradigm systems and high-level general purpose language scripts.

UNIT I LINUX ESSENTIALS 9

ntroduction to Linux- File system of the Linux- General usage of Linux kernel 7 basic commands- Linux users and group- Permissions for file- directory and users- Searching a file & directory- Zipping and unzipping concepts

UNIT II FUNDAMENTALS TO SCRIPTS AND PERL LANGUAGE 9

Characteristics and uses of scripting languages - Introduction to PERL- Names and values - Variables and assignment - Scalar expressions - File handles – Operators - Control structures - Regular expressions - Built in data types - Statements and declarations – simple – Compound - Loop statements - Global and scoped declarations

UNIT III PERL SCRIPTING 9

PERL built-in functions- Collections of data- Working with arrays- Lists and hashes – Simple input and output – Strings - Patterns and regular expressions- Subroutines- Scripts with arguments

UNIT IV TCL RUDIMENTS 9

TCL fundamentals- String and pattern matching- Structure Syntax - Parser- Variables and data in TCL- Control flow- Data structures- Simple input/output- Procedures and scope- Working with strings- Patterns- Files and pipes- Example code

UNIT V AUXILIARY LANGUAGES 9

JavaScript - Object models- Design philosophy- Versions of JavaScript- The Java Script core language- Introduction to Python- Using the Python interpreter- More control flow tools- Data structures- Modules- Input and output- Errors and Exceptions- Classes- Brief Tour of the standard library

Contact Periods:

Lecture : 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. David Barron, "The World of Scripting Languages", 1st edition, Wiley Publication, 2000
2. Randal L, Schwartz Tom Phoenix, "Learning PERL", 3rd edition, Oreilly Publications, 2001

REFERENCES:

1. Tom Christiansen, Brian D Foy, Larry Wall, and John Orwant, "Programming Perl", 4th edition, O'Reilly Media, Inc. Publishers, 2012.
2. M.Lutz,SPD, "Programming Python", 4th edition, O'Reilly Media, Inc. Publishers, 2010
3. Steve Holden and David Beazley, "Python Web Programming", 1st edition, New Riders Publications, 2002
4. J.Lee and B.Ware ,"Open Source Web Development with LAMP using Linux Apache, MySQL, Perl and PHP", 1st edition, Addison Wesley Professional Publisher, 2002

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Explain basic commands of Linux to work in Linux environment	Understand
CO2	Illustrate elementary commands of PERL in system design	Understand
CO3	Examine the scripts involved in PERL language	Analyze
CO4	Make use of scripts to run in TCL environment	Apply
CO5	Summarise basics of JAVA and PYTHON scripts	Understand

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	3	3	3	-	-	2
CO4	3	2	3	-	-	1
CO5	2	1	1	-	-	-
CO	2	2	2	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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P21VLP06	SYSTEM VERILOG	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Data Structures

COURSE OBJECTIVES:

- To understand the basic concepts of verilog
- To learn different statements and interfaces of system verilog
- To apply system Verilog programming for real time application

UNIT I BASICS OF SYSTEM VERILOG 9

Introduction to System Verilog – Packages – Declarations – Simulation Time Units – Precision – Variables – Data Types

UNIT II DATA STRUCTURES 9

Structures – Declarations – Packed Structures – Passing Structures – Unions – Packed, Unpacked, Tagged Unions - Arrays – Array Operation

UNIT III STATEMENTS AND CONTROL STRUCTURES 9

Procedural Blocks – Combinational, Sequential and Latched Logic – Enhancements to Tasks and Functions – Operand Enhancements – New Jump Statements – Enhanced Case Statements – Enhanced if else Decision

UNIT IV MODULES AND INTERFACES 9

Module Prototypes – Declaration – Instances – Net Aliasing – Interface Concepts – Global and Local Interfaces – Interface Ports – Connecting Interfaces – Mode Ports

UNIT V SYSTEM MODELLING 9

State Machine Modelling – ATM Example – Transmitter and Receiver – Test Benches – Memories of System – Complex Transactions

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Simon Davidmann,"System Verilog for Design",2nd edition,2003
2. T.Kropf, "Introduction to Formal Hardware Verification", 7th edition, Springer Verlag, 2010

REFERENCES:

1. Janick Bergeron, "Writing Test Benches Functional Verification of HDL Models",3rd edition, Springer, 2003
2. Andreas Meyer, "Principles of Functional Verification", 5th edition, Newness, 2003
3. Chris Spear, "System Verilog for Verification: A Guide to Learning the Test bench Language Features", 5th edition, Springer, 2008
4. Janick Bergeron, Edward Cerny, Alan Hunter and Andrew Nightingale, "Verification Methodology Manual for System Verilog", 3rd edition, Springer, 2005

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Explain the basic concepts of Verilog	Understand
CO2	Illustrate the operations of data structures	Understand
CO3	Make use of procedural statements in system Verilog programming	Apply
CO4	Summarize the different modules and interface of system Verilog	Understand
CO5	Implement real time applications using system Verilog	Analyze

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	3	2	3	-	-	1
CO4	2	1	1	-	-	-
CO5	3	3	3	-	-	2
CO	2	2	2	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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ELECTIVE–III

P21VLP07	DESIGN OF SEMICONDUCTOR MEMORIES	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Digital CMOS VLSI Design
- Semiconductor device Modeling

COURSE OBJECTIVES:

- To study the concepts of MOS and nonvolatile memories architecture and its operations.
- To analyze various testing methods of semiconductor memories.
- To understand reliability and advanced packaging technologies of semiconductor memories.

UNIT I RANDOM ACCESS MEMORY TECHNOLOGIES 9

SRAM cell structures - MOS SRAM architectures, MOS SRAM cell, Bipolar SRAM technologies, Silicon On Insulator (SOI) technology, advanced SRAM architectures and technologies.

DRAM technology development - CMOS DRAMs, DRAMs cell theory, BiCMOS, DRAMs, soft error failures in DRAMs, advanced DRAM designs and architectures

UNIT II NONVOLATILE MEMORIES 9

Masked Read-Only Memories (ROMs) - High density ROMs. Programmable Read-Only Memories (PROMs) - Bipolar PROMs, CMOS PROMs. EPROMs - Floating-Gate EPROM Cell, One-Time Programmable (OTP). EEPROMs - EEPROM technology and architectures, non-volatile SRAM. Flash memories (EPROMs or EEPROM) - advanced flash memory architectures

UNIT III MEMORY FAULT MODELING AND TESTING 9

RAM fault modeling - Electrical testing - Pseudo random testing - Megabit DRAM testing non-volatile memory modeling and testing - IDDQ fault modeling and testing - Application specific memory testing

UNIT IV SEMICONDUCTOR MEMORY RELIABILITY 9

General Reliability Issues-RAM Failure Modes and Mechanism-Non-volatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification

UNIT V ADVANCED MEMORY TECHNOLOGIES 9

Ferroelectric Random Access Memories (FRAMs) - Gallium Arsenide (GaAs) FRAMs - Analog memories - Magneto-resistive Random Access Memories (MRAMs) - Memory hybrids and MCMs (2D) - Memory stacks and MCMs (3D) - Memory MCM testing and reliability Issues - Memory cards - High density memory packaging future directions

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Ashok.K.Sharma, "Semiconductor Memories: Technology, Testing and Reliability", Wiley IEEE press, New York, 2002.
2. Brent Keeth, R. Jacob Baker, Brian Johnson, Freng Lin, "DRAM Circuit Design: Fundamental and High Speed Topics", Wiley-IEEE Press, 2nd Edition, 2008.

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REFERENCES:

1. Ashok K. Sharma, "Semiconductor Memories", Two-Volume Set, Wiley-IEEE Press, 2003
2. Betty Prince, "High Performance Memories: New Architecture DRAMs and SRAMs – Evolution and Function", Wiley, Revised Edition, 1999
3. Sharma, Ashok K., "Semiconductor Memories: Technology, Testing, and Reliability", Wiley- IEEE Press, New York, 2002
4. Tegze P. Haraszti, "CMOS Memory Circuits", Kluwer Academic publishers, 2002 Edition, 2007

COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Illustrate the micro level operations of Random Access Memories	Understand
CO2	Explain the need of non-volatile memories and their applications	Understand
CO3	Analyze the fault free memory systems by fault modeling techniques	Analyze
CO4	Outline the reliability and radiation effects of memory	Understand
CO5	Summarized the concepts of advanced packaging technologies for semiconductor memories	Understand

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	3	3	3	-	-	2
CO4	2	1	1	-	-	-
CO5	2	1	1	-	-	-
CO	2	2	2	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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P21VLP08	SEMICONDUCTOR DEVICE MODELLING	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Semiconductor Physics and Devices

COURSE OBJECTIVES:

- To learn about device modeling and design parameters of MOSFET
- To acquaint performance parameters of CMOS device
- To understand the concepts of bipolar device models

UNIT I MOSFET DEVICE PHYSICS 9

Capacitances in MOS structure – Poly–silicon gate work function and depletion effects – Charge in silicon dioxide – Effect of interface traps and oxide charge on device characteristics – Impact ionization and avalanche Breakdown – Band-to-band tunneling in MOSFET – Injection of hot carriers High–field effects in gated diode

UNIT II DEVICE MODELING 9

Long channel MOSFETs – Sub–threshold characteristics – Short channel MOSFETs – Velocity saturation and high–field transport channel length modulation – MOSFET degradation and breakdown at high fields – Device simulations in VLSI – Nodal, mesh, modified nodal and hybrid analysis equations – Solution of nonlinear networks through Newton-Raphson technique – Convergence and stability

UNIT III DEVICE DESIGN 9

MOSFET Scaling – Constant–field scaling – Generalized scaling – Non–scaling effects – Threshold voltage requirement – Channel Profile Design – Non-uniform doping – Quantum effect on threshold voltage – Discrete dopant effects on threshold voltage – MOSFET channel length – Extraction of effective channel length by C-V measurements

UNIT IV CMOS PERFORMANCE FACTORS 9

CMOS parasitic elements – Source–drain resistance, parasitic capacitances, gate resistance, interconnect R and C – Sensitivity of CMOS delay to device parameters – Delay sensitivity to channel Width, Length, and gate oxide thickness, supply voltage and threshold voltage – Sensitivity of delay to parasitic resistance and capacitance – Performance factors of advanced CMOS devices

UNIT V BIPOLAR DEVICE MODELS 9

Ideal current - voltage Characteristics – Effect of emitter and base series resistances – Effect of base – collector voltage on collector current – Collector current fall–off at high currents – Bipolar device models for circuit and time-dependent analyses – Basic dc model, basic ac Model, small-signal equivalent circuit model – Emitter diffusion capacitance – Charge-control analysis – Breakdown voltages – SPICE models

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Yuan Taur, TakH Ning, "Fundamentals of Modern VLSI Devices", 2nd edition, Cambridge University Press, 2013
2. B.G Streetman and S.K Banerjee, "Solid State Electronic Devices", 7th edition, Prentice Hall India, 2015

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REFERENCES:

1. J P Collinge, C A Collinge, "Physics of Semiconductor Devices" 2nd edition, Springer, 2006
2. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly Wayne Wolf, "Device Modeling for Analog and RFCMOS Circuit Design", 1st edition, John Wiley & Sons Ltd., 2003
3. S.M. Sze Kwok K. Ng, "Physics of Semiconductor Devices", 2nd edition, John Wiley & Sons, 2007
4. Arora, Narain D. "Fundamentals of Microelectronics", 2nd edition, Wiley Student Edition, 20013

COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Examine the parasitic effects in MOSFET device	Analyze
CO2	Choose the suitable technique for device modeling	Apply
CO3	Explain the concepts of scaling and threshold effects in MOSFET	Understand
CO4	Analyze the performance parameters of CMOS device	Analyze
CO5	Interpret the characteristics of bipolar device models	Understand

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	-	-	2
CO2	3	2	3	-	-	1
CO3	2	1	1	-	-	-
CO4	3	3	3	-	-	2
CO5	2	1	1	-	-	-
CO	3	2	2	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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P21VLP09	INTERCONNECTION AND PACKAGING FOR VLSI	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- VLSI Design

COURSE OBJECTIVES:

- To study the interconnections and its advancements
- To understand the parameters associated with interconnects
- To learn the IC packaging process

UNIT I INTERCONNECTIONS FOR VLSI APPLICATIONS 9

Metallic interconnections – Multilevel, multilayer and multipath configurations – Optical interconnections – Superconducting interconnections – Copper interconnections – Advantages of copper interconnects – Challenges posed by copper interconnects – Fabrication processes for copper interconnects – Damascene processing of copper interconnects – Miller's theorem

UNIT II INTERCONNECTION PARAMETERS 9

Parasitic resistances – General considerations – Parasitic capacitances – General considerations – Parallel–Plate capacitance – Fringing capacitances – Coupling Capacitances – Parasitic Inductances – General considerations – Self and mutual inductances – Partial inductances – Methods for inductance extraction – Effect of inductances on interconnection delay

UNIT III FUTURE INTERCONNECTION 9

Optical interconnections – Transmission line models of lossy optical waveguide interconnections – Superconducting interconnections – Nanotechnology circuit interconnections

UNIT IV SINGLE CHIP PACKAGING 9

Trends in IC packaging – Area array packages – PGA, BGA – BGA surface mount assembly – BGA attributes

UNIT V MULTICHIP PACKAGING 9

MCP substrate/Package technologies – Hybrid circuit – Multichip module – 3D Packaging and the flex circuit – Die stacking using silicon Thru–Vias – System in Package (SiP)/System on Package (SoP)

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1 Ashok K Goel, "High–Speed VLSI Interconnections", 2nd edition, Wiley–Interscience, IEEE Press, 2007
2 Hartmut Grabinski, "Interconnects in VLSI Design", 1st edition, Springer Science, 2000

REFERENCES:

1 William Greig, "Integrated Circuit Packaging: Assembly and Interconnections", 1st edition, Springer Series in Advanced Microelectronics, 2010
2 Francesc Moll and Miquel Roca, "Interconnection noise in VLSI Circuits", 1st edition, Kluwar Academic Publishers, 2012
3 H. B. Bakoglu, "Circuits, Interconnections, and Packaging for VLSI", 1st edition, Addison Wesley Longman, 1990

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Summarize the different types of interconnections and its applications	Understand
CO2	Examine the performance of various parameters associated with interconnections	Analyze
CO3	Identify the appropriate future interconnections for VLSI circuits	Apply
CO4	Explain the single chip packaging processes of VLSI system	Understand
CO5	Illustrate the process of multi–chip packaging of VLSI system	Understand

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	3	3	3	-	-	2
CO3	3	2	3	-	-	1
CO4	2	1	1	-	-	-
CO5	2	1	1	-	-	-
CO	2	2	2	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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ELECTIVE-IV

P21VLP10	HARDWARE VERIFICATION TECHNIQUES	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Fundamentals of testing

COURSE OBJECTIVES:

- To understand the concepts of verification techniques and tools
- To study the strategies of verification and stimulus
- To learn the basics of testbenches, functional and quality verification
-

UNIT I VERIFICATION TECHNIQUES AND TOOLS 9

Testing vs Verification – Design and verification – Functional verification approaches – Formal verification – Linting tools – Simulators – Waveform viewers – Code coverage – Tracking metrics

UNIT II VERIFICATION PLAN 9

Role of verification plan – Levels of verification – Verification strategies – Specification and features – Directed testbenches approach

UNIT III STIMULUS AND RESPONSE 9

Simple stimulus – Simple output – Complex stimulus – Bus functional models – Response monitors – Transaction level interface

UNIT IV ARCHITECTING TESTBENCHES 9

Test harness – VHDL test harness – Design configuration – Self-checking testbenches – Directed stimulus – Random stimulus

UNIT V FUNCTIONAL AND QUALITY VERIFICATION 9

Project costs – Methodology – Tools - Structuring a project – Project management – Estimating quality – Overview of methods

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS

1. Janick Bergeron, "Writing Testbenches: Functional Verification of HDL Models", 2nd edition, Springer, 2003
2. Andreas Meyer, "Principles of Functional Verification", 1st edition, Newnes, 2003

REFERENCES

1. Samir Palnitkar, "Design Verification with E",PHI, 2003
2. Thomas Kropf, "Introduction to Formal Hardware Verification", Springer, 2010
3. Chris Spear, "System Verilog for Verification: A Guide to Learning the Testbench language Features", Springer, 2008
4. Janick Bergeron, Edward Cerny, Alan Hunter and Andrew Nightingale, "Verification Methodology Manual for System Verilog", Springer, 2005

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Explain the various techniques and tools used for verification	Understand
CO2	Summarize different verification levels and strategies	Understand
CO3	Compare the performance of simple and complex stimulus	Understand
CO4	Develop testbenches using different stimuli	Apply
CO5	Examine the quality and functionality of a project	Analyze

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	2	1	1	-	-	-
CO4	3	2	3	-	-	1
CO5	3	3	3	-	-	2
CO	2	2	2	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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P21VLP11	IP BASED VLSI	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Security Protocols

COURSE OBJECTIVES:

- To understand the various IC manufacturing and IP based fabrication techniques
- To design the IP based combinational, sequential and subsystem blocks
- To learn floor planning and IP design security

UNIT I DIGITAL SYSTEM AND IP BASED VLSI FABRICATION 9

Introduction – IC manufacturing – CMOS technology – IC design techniques – IP based design – Fabrication process –Transistors – Wires and Via – Fabrication theory – Reliability – Layout design and tools

UNIT II IP BASED COMBINATIONAL LOGIC NETWORKS 9

Combinational logic functions – Static complementary gates – Switch logic – Low power gates – Delay – Design for yield – Gates as IP – Standard cell-based layout – Combinational network delay – Logic and interconnect design – Power optimization – Switch logic networks – Logic testing

UNIT III SEQUENTIAL AND SUBSYSTEM DESIGN USING IP 9

Latch and flip flops – Sequential system and clocking – Performance analysis – Power optimization – Design validation – Testing – Combinational shifter – Arithmetic Circuits – High density memory – Image sensors – Buses and NoC – Subsystems as IP

UNIT IV IP FLOOR PLANNING AND ARCHITECTURE DESIGN 9

Floor planning methods – Global interconnect – Floorplan design – Off–chip connections – Register transfer design – High level synthesis – Architecture for low power – GALS systems – Architecture testing – IP components – Design methodologies – Multiprocessor System–on–chip Design

UNIT V DESIGN SECURITY 9

IP in reuse based design – Constrained based IP protection – Protection of data and privacy – Constrained based watermarking for VLSI IP based protection

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Wayne wolf, "Modern VLSI Design: IP–based Design", 4th edition, Pearson Education, 2015
2. Gang Qu and Miodrag potkonjak, "Intellectual Property Protection in VLSI Designs: Theory and Practice", 3rd edition, Kluwer Academic Publishers,2003

REFERENCES:

1. Gerald R. Peterson and Fredrick J. Hill," Computer Aided Logical Design with Emphasis on VLSI", 4th Edition, Wiley,2020
2. Thomas E. Dillinger," VLSI Design Methodology Development", 2nd edition, Pearson education,2019
3. Jan M Rabaey, "Digital Integrated Circuits: A Design", 2nd edition, PHI,2016

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Summarize various IP based IC fabrication techniques	Understand
CO2	Examine the performance of IP based combinational logic network	Analyze
CO3	Interpret the various IP based sequential and subsystem design	Understand
CO4	Infer architecture and IP based floor planning design of low power circuits	Understand
CO5	Identify the suitable protection method for securing VLSI design	Apply

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	3	3	3	-	-	2
CO3	2	1	1	-	-	-
CO4	2	1	1	-	-	-
CO5	3	2	3	-	-	1
CO	2	2	2	-	-	2

Correlation levels: 1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High)

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P21VLP12	VLSI FOR WIRELESS COMMUNICATION	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- VLSI Design
- Digital Communication

COURSE OBJECTIVES:

- To learn the basic concept of wireless communication
- To study transmitter and receiver architectures of VLSI for wireless communication
- To understand frequency synthesizer and types of mixers

UNIT I BASIC CONCEPTS OF WIRELESS COMMUNICATION 9

Overview of wireless systems-access methods-modulation schemes-wireless channel description-path loss- multipath fading-channel model-envelope-frequency selective and fast fading

UNIT II TRANSMITTER ARCHITECTURES AND POWER AMPLIFIER 9

Transmitter block end- design philosophy- direct conversion and other architectures- quadrature LO generator- single ended RC- single ended LC- RC with differential stages- divider based generator, power amplifier design-PA design issues-Class A, AB/B/C,E amplifiers

UNIT III ACTIVE AND PASSIVE MIXER 9

Balancing-low frequency and high frequency case analysis- switching mixer- distortion in unbalanced switching mixer- single ended sampling mixer- conversion gain, noise, sampling mixer, distortion, intrinsic and extrinsic noise.

UNIT IV FREQUENCY SYNTHESIZER 9

PLL based frequency synthesizer- phase detector- dividers- Oscillators- Loop filter- first order, second order- high order filters- design approaches- implementation of a frequency synthesizer with a fractional divider.

UNIT V RECEIVER ARCHITECTURES 9

Receiver front end- filter design- low noise amplifier- wideband LNA design- narrow band LNA-impedance matching- core amplifier.

Contact Periods:

Lecture: 45 Periods Tutorial: - Periods Practical: – Periods Total: 45 Periods

REFERENCES:

1. Bosco Leung, "VLSI for Wireless Communication", 2nd edition, Springer publications, Canada, 2011.
2. David Tse and Pramod Viswanath, "Fundamentals of Wireless Communication", 1st edition, Cambridge Press, 2005.
3. DALAL & UPENA, "Wireless Communication", 1st edition, Oxford University Press, New Delhi, 2014.
4. Carols and M. Stewart, "CMOS Wireless Transceiver Design," 1st edition, Boston, Kluwer Academic Publication, 2005
5. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits', 1st edition, Cambridge University Press, 2003.

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Outline the concepts of wireless communication system	Understand
CO2	Explain different modules in transmitter architectures	Understand
CO3	Make use of active and passive mixer for VLSI circuits	Apply
CO4	Analyze different phase and frequency processing components	Analyze
CO5	Illustrate the various receiver architecture	Understand

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	3	2	3	-	-	1
CO4	3	3	3	-	-	2
CO5	2	1	1	-	-	-
CO	2	2	2	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)		3: Substantial (High)	

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ELECTIVE-V

P21VLP13	ARM PROCESSOR AND APPLICATIONS	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Embedded Systems

COURSE OBJECTIVES:

- To study the architecture and assembly language programming of ARM processor
- To learn the data types and memory management
- To understand the architectural support for system development and operating system

UNIT I ARM ARCHITECTURE 9

Abstraction in hardware design – MUO – Acorn RISC machine – Architecture inheritance – ARM programming model – ARM development tools – 3 and 5 Stage pipeline ARM organization – ARM instruction execution and implementation – ARM co-processor interface

UNIT II ASSEMBLY LANGUAGE PROGRAMMING 9

ARM instruction types – Data transfer, data processing and control flow instructions – ARM instruction set – Co–processor instruction – Assembly language programming

UNIT III HIGH LEVEL LANGUAGE AND MEMORY HIERARCHY 9

Data types – Abstraction in software design – Expressions – Loops – Functions and procedures – Conditional statements – Use of memory – Memory size and speed – On chip memory – Cache design – Memory management

UNIT IV ARCHITECTURAL SUPPORT FOR SYSTEM DEVELOPMENT 9

Microcontroller bus architecture – ARM memory interface – ARM reference peripheral specification – Hardware system prototyping tools – Emulator – Debug architecture

UNIT V ARCHITECTURAL SUPPORT FOR OPERATING SYSTEM 9

ARM system control coprocessor – CP15 protection unit registers – ARM protection unit – CP15 MMU registers – ARM MMU architecture – Synchronization – Context switching – Input and output – Case study – Chocolate Vending Machine

Contact Periods:

Lecture: 45 Periods Tutorial: –Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Steve B Furber, "ARM System on Chip Architecture", 2nd edition, Pearson Education, 2015
2. Ata Elahi and Trevor Arjeski, "ARM Assembly Language with Hardware Experiments", 1st edition, Springer, 2014.

REFERENCES:

1. Muhammad Ali Mazidi and Sarmad Naimi, "ARM Assembly Language Programming and Architecture", 2nd edition, Microdigital education, 2019
2. Ricardo Reis and Jochen A.G, "Design of System on a Chip: Devices and Components", 1st edition, Springer, 2004
3. William Hohl and Christopher Hinds, "ARM Assembly Language: Fundamentals and Techniques", 2nd edition, CRC Press, 2014
4. Bob Zeidman, "Designing with FPGAs and CPLDs", 4th edition, Elsevier, CMP Books, 2002

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Interpret different types of ARM architectures	Understand
CO2	Choose the appropriate instructions for assembly language programming	Apply
CO3	Infer the high -level language and memory hierarchy	Understand
CO4	Explain the architectural support for system development	Understand
CO5	Examine the performance of operating system for real time application	Analyze

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	3	2	3	-	-	1
CO3	2	1	1	-	-	-
CO4	2	1	1	-	-	-
CO5	3	3	3	-	-	2
CO	2	2	2	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)			3: Substantial (High)

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P21VLP14	INDUSTRIAL INTERNET OF THINGS	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Computer Networks

COURSE OBJECTIVES:

- To learn fundamentals of Internet of Things (IoT)
- To understand the IoT protocol standards and hardware designs
- To apply the concepts of IoT in real-time applications

UNIT I FUNDAMENTALS OF IoT 9

IoT – Physical design – Logical design – IoT enabling technologies – IoT levels and deployment templates – Domain specific IoTs – IoT and M2M – communication models and APIs

UNIT II IoT ARCHITECTURE 9

M2M high–level ETSI architecture – IETF architecture – OGC architecture – IoT reference model – Domain model – Information model – Functional model – Communication model – IoT reference architecture

UNIT III IoT PROTOCOLS 9

Protocol standardization for IoT – M2M and WSN protocols – SCADA and RFID protocols – Unified Data Standards (UDS) Protocols – IEEE 802.15.4 – BACNet protocol – Modbus – Zigbee architecture – Network layer – 6LowPAN – CoAP – Security

UNIT IV BUILDING IoT WITH RASPBERRY PI 9

Building IoT with Raspberry Pi – IoT Systems – Logical design using python – IoT physical devices and endpoints – IoT Device – Building blocks – Raspberry Pi board – Raspberry Pi interfaces – Programming Raspberry Pi with python

UNIT V CASE STUDIES AND REAL WORLD APPLICATIONS 9

Real world design constraints – Applications – Asset management, industrial automation, smart grid, commercial building automation, smart cities – Participatory sensing – Data analytics for IoT software, management tools for IoT cloud storage models, communication APIs – Cloud for IoT

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Arshdeep Bahga, Vijay Madisetti, "Internet of Things: A hands–on approach", 1st edition, Universities Press, 2015
2. Olivier Hersent, David Boswarthick, Omar Elloumi, "The Internet of Things –Key applications and Protocols", 1st edition, Wiley, 2015

REFERENCES:

1. Honbo Zhou, "The Internet of Things in the Cloud: A Middleware Perspective", 1st edition, CRC Press, 2012
2. Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Avesand, David Boyle, "From Machine–to–Machine to the Internet of Things – Introduction to a New Age of Intelligence", 1st edition, Elsevier, 2014
3. Dieter Uckelmann, Mark Harrison, Michahelles, Florian (Eds), "Architecting the Internet of Things", Springer, 2011

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4. Hanes David , Salgueiro Gonzalo, Grossetete Patrick, Barton Rob, Henry Jerome, "IoT Fundamentals: Networking Technologies, Protocols and Use Cases for the Internet of Things", 1st edition, Pearson Education, 2017

COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Illustrate the basics of Internet of Things and its levels	Understand
CO2	Infer different IoT architecture design related to real–time applications	Understand
CO3	Interpret the different IoT communication protocols	Understand
CO4	Examine the performance of various Raspberry Pi interfaces for simple applications	Analyze
CO5	Solve a real-world problem using the concept of Industrial Internet of Things	Apply

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	2	1	1	-	-	-
CO4	3	3	3	-	-	2
CO5	3	2	3	-	-	1
CO	2	2	2	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)			3: Substantial (High)

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P21VLP15	SECURITY SOLUTIONS IN VLSI	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Network Security

COURSE OBJECTIVES:

- To understand the different kinds of threats in VLSI
- To acquaint knowledge about security counter measure and reconfigurable computing
- To study various hardware-based security challenges and solutions

UNIT I FUNDAMENTALS OF SECURITY 9

Security attacks – Security services – Security mechanisms – Security model – Threats to Security – Physical security – Biometric systems – Monitoring controls – Data security – Computer System security – Communication security

UNIT II SECURITY COUNTER MEASURES 9

Types of firewalls – Comparison of firewall types – Firewall configurations – Intrusion detection and prevention systems – Privacy concepts – Privacy principles and policies – Authentication and privacy – Privacy impacts of emerging technologies

UNIT III RECONFIGURABLE COMPUTING 9

Reconfigurable computing system – PAM – VCC – Splash – PRISM – Teramac – Cray – SRC – Non-FPGA – Reconfiguration Management – Reconfiguration – Configuration architectures – Managing reconfiguration process – Reducing reconfiguration time – Configuration security

UNIT IV SECURITY CHALLENGES IN VLSI 9

Recent security issues – Case study – Testability issues in modern VLSI – Superscalar architecture – Intel Pentium processor – Hardware security challenges beyond CMOS

UNIT V CRYPTO CHIP DESIGN AND HARDWARE SECURITY 9

VLSI Implementation of AES algorithm – Implementation of DES – Development of digital signature chip using RSA algorithm – Hardware based security solution – Hardware Accelerators – Security Enhancement techniques – Hardware Trojans

Contact Periods:

Lecture: 45 Periods Tutorial: - Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Charels P. P fleeger "Security in Computing", 1st edition, PHI, 2006
2. Wayne wolf, "Modern VLSI Design:IP-based Design", 4th edition, Pearson Education,2009

REFERENCES:

1. Bobda Christophe, "Introduction to Reconfigurable Computing: Architectures, Algorithms, and Applications", 1st edition, Springer, 2007
2. Hauck Scott, Dehon A, "Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation", 1st edition, Elsevier, 2007
3. William Stalling "Cryptography and Network Security", 4th edition, Pearson Education, 2005
4. Jeff Crume "Inside Internet Security", 1st edition, Addison Wesley, 2000

COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Explain the basic concept of security mechanism	Understand
CO2	Examine the different security prevention methods	Analyze
CO3	Make use of reconfigurable system in recent application domains	Apply
CO4	Infer the security challenges in VLSI	Understand
CO5	Choose the appropriate cryptography algorithms for hardware security.	Apply

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	3	3	3	-	-	2
CO3	3	2	3	-	-	1
CO4	2	1	1	-	-	-
CO5	3	2	3	-	-	1
CO	2	2	2	-	-	1
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)			3: Substantial (High)

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ELECTIVES VI

P21VLP16	THERMAL ANALYSIS AND POWER MANAGEMENT OF INTEGRATED CIRCUITS	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Nil

COURSE OBJECTIVES:

- To understand about thermal issues in CMOS
- To learn testing and modeling of IC for thermal conditions
- To study the basics behind characteristics and thermal designing of VLSI circuits

UNIT I THERMAL ISSUES IN VLSI CIRCUITS 9

Evolution of CMOS technology – Electro thermal phenomena in VLSI systems – Electro thermal Simulation – Emergence of thermal issues – Power in nanometer regime – Leakage reduction techniques junction temperature projections – Reliability issues in scaled technologies

UNIT II TESTING ICs FOR NORMAL OPERATING CONDITIONS 9

Burn-in test – Temperature and voltage acceleration factors – Technology scaling and burn-in – Burn-in elimination – Estimation of junction temperature – Packaging considerations for burn-in – Cooling techniques for burn-in – Burn-in limitations and optimization

UNIT III THERMAL AND ELECTRO THERMAL MODELING 9

Objectives of thermal analysis – Thermal network modeling – Architectural level Electro thermal modeling – Electro thermal modeling at logic level – Electro thermal modeling at circuit level – Electro thermal modeling at device level

UNIT IV THERMAL RUNAWAY AND THERMAL MANAGEMENT 9

Thermal awareness – Thermal runaway: Thermal runaway during burn-in-thermal management, during normal operating conditions – Temperature management: a case study – Temperature measurement of semiconductor devices

UNIT V LOW TEMPERATURE CMOS OPERATION 9

Low temperature motivation – Low temperature characterization of CMOS devices – Reliability at low temperature – Microprocessor low temperature operation: A Case Study – Disadvantages of low temperature electronic cooling – Cooling technologies – Temperature dependent MOS device modeling introduction – Temperature dependent device physics and modeling – Region Wise Quadratic (RWQ) model

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Yi-Kan Cheng, Ching-Han Tsai, Chin-Chi Teng and Sung-Mo Kang, , "Electro Thermal Analysis of VLSI Systems", 3rd edition, Kluwer Academic Publishers, 2002
2. Arman Vassighi and Manoj Sachdev, "Thermal and Power Management of Integrated Circuits", 2nd edition, Springer, 2006

REFERENCES:

1. Mona M. Hella, Patrick Mercier, "Power management Integrated Circuits", 1st edition, CRC Press, 2018

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2. Phillip E. Allan, Douglas R. Holberg, "CMOS Analog Circuit Design", 2nd edition, Oxford University Press, 2002
3. N.K. Jha, Sandeep Gupta, "Testing of Digital Systems", 4th edition, Cambridge University Press, 2012

COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K-Level
CO1	Explain various thermal issues of VLSI circuits	Understand
CO2	Examine the IC operation through testing under various conditions	Analyze
CO3	Analyze the thermal and electro thermal modeling at different levels	Analyze
CO4	Identify thermal runaway problems of semiconductor devices	Apply
CO5	Summarize different CMOS operations at low temperature	Understand

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	3	3	3	-	-	2
CO3	3	3	3	-	-	2
CO4	3	2	3	-	-	1
CO5	2	1	1	-	-	-
CO	3	2	2	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)			3: Substantial (High)

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P21VLP17	OPTIMIZATION ALGORITHM FOR VLSI	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:

- Basics of optimization algorithm

COURSE OBJECTIVES:

- To learn basic concept of optimization algorithm
- To study optimization algorithm based on neural networks, fuzzy and genetic algorithms
- To understand ant colony optimization and particle swarm optimization

UNIT I NATURE INSPIRED ALGORITHMS 9

Introduction to algorithm – Newton's method – Optimization algorithm – No-free-lunch theorems – Nature – Inspired meta heuristics – Analysis of algorithms – Parameter tuning and parameter control.

UNIT II NEURAL NETWORKS AND FUZZY LOGIC SYSTEMS 9

Neural network – Back propagation network, Generalized delta rule – Radial basis function network– Interpolation and approximation RBFNS – Comparison between RBFN and BPN. Basic of fuzzy logic theory – Crisp and fuzzy sets – Basic set operation– Neuro-Fuzzy modelling – Adaptive Neuro – Fuzzy Inference System (ANFIS) – ANFIS architecture – Hybrid learning algorithm

UNIT III EVOLUTIONARY COMPUTATION AND GENETIC ALGORITHMS 9

Evolutionary computation (EC) – Features of EC, classification of EC, advantages, applications– Introduction of Genetic algorithms – Biological background – Operators in GA-GA algorithm– Classification of GA, applications.

UNIT IV ANT COLONY OPTIMIZATION 9

Introduction from real to artificial ants – Theoretical considerations – Convergence proofs – ACO algorithm – ACO and model–based search – Application principles of ACO

UNIT V PARTICLE SWARM OPTIMIZATION 9

Introduction – Principles of bird flocking and fish schooling – Evolution of PSO – Operating principles – PSO algorithm – Neighbourhood topologies – Convergence criteria – Applications of PSO– Honey bee social foraging algorithms – Bacterial foraging optimization algorithm

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOKS:

1. Eiben, A.E. Smith and James E, "Introduction to Evolutionary Computing", 2nd edition, Springer 2015
2. Helio J.C. Barbosa, "Ant Colony Optimization – Techniques and Applications", 1st edition, Intech 2013

REFERENCES:

1. Christopher M. Bishop, "Neural Networks for Pattern Recognition", 1st edition, Oxford University Press 1995
2. Nello Cristianini, John Shawe, Taylor, "An Introduction to Support Vector Machines and Other Kernel– based Learning Methods", 2nd edition, Cambridge University Press 2013
3. Bhuvaneswari M.C, "Application of Evolutionary Algorithms for Multi–objective Optimization in VLSI and Embedded Systems", 1st edition, Springer 2015
4. Pakize Erdogmus "Particle Swarm Optimization with Applications", 1st edition, Duzce University, Intech 2018

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COURSE OUTCOMES:

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Explain the basic concept of optimization algorithm	Understand
CO2	Illustrate the neural networks and fuzzy logic optimization algorithm	Understand
CO3	Interpret the basic concept of evolutionary computation and genetic algorithms	Understand
CO4	Examine the performance of ant colony algorithm	Analyze
CO5	Apply the ACO algorithm for real time application	Apply

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	2	1	1	-	-	-
CO4	3	3	3	-	-	2
CO5	3	2	3	-	-	1
CO	2	2	2	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)			3: Substantial (High)

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P21VLP18	MEMS AND NEMS	Category: PEC			
		L	T	P	C
		3	0	0	3

PRE–REQUISITES:
- RF MEMS

COURSE OBJECTIVES
- To understand the fabrication of microsystems and its electrical and mechanical concepts
- To learn the fundamentals of micro-sensors and system issues of micro circuits
- To study different levels of MEMS Packaging

UNIT I BASICS OF MICRO FABRICATION 9

Overview – Wafer level process – Substrates – Wafer cleaning – Oxidation of Silicon – Local oxidation –Doping – Thin-film deposition – Wafer bonding pattern transfer – Optical lithography – Design rules – Mask making – Wet etching – Dry etching – Additive process – Planarization

UNIT II ELECTRICAL AND MECHANICAL CONCEPTS 9

Conductivity of semiconductors – Crystal planes and orientations – Stress and strain – Flexural beam bending analysis using simple loading conditions – Torsional deflection– Intrinsic stress – Dynamic system – Resonance frequency – Quality factor – Active tuning of spring constant and resonant frequency

UNIT III ELECTRO STATIC SENSING AND ACTUATION 9

Introduction to electrostatic sensors and actuators – parallel-plate capacitor – Application of parallel plate capacitors – Interdigitated finger capacitors – Application of comb drive devices

UNIT IV CIRCUIT AND SYSTEM ISSUES 9

Electronics: Introduction – Elements of semiconductor physics – MOSFET– MOSFET amplifiers – Operational amplifiers – Dynamic effects – Basic op–amp circuits – Charge measuring circuits – Noise: The interference problem – Characterization of signals – Characterization of random noise – Noise sources

UNIT V MICRO SYSTEM PACKAGING AND NANO DEVICES 9

General considerations in packaging – The three levels of micro system packaging – Die level – Device level and system level – Essential packaging technologies – Die preparation – Three-dimensional packaging – Assembly of Microsystems – Atomic Structures and Quantum Mechanics – Schrodinger Equation – ZnO nanorods based NEMS device – Gas sensor

Contact Periods:

Lecture: 45 Periods Tutorial: – Periods Practical: – Periods Total: 45 Periods

TEXT BOOK
1. Chang Liu, "Foundations of MEMS", 2nd edition, Pearson India, 2016
2. Cornelius T. Leondes, "MEMS/NEMS Handbook– Techniques and Applications", 2nd edition, Springer Publication, 2006

REFERENCES
1. Marc J. Madou, "Fundamentals of Microfabrication and Nanotechnology", 3rd edition, Taylor & Francis, 2011
2. Tai– Ran Hsu, "MEMS and MicroSystems: Design Manufacture and Nanoscale engineering", 2nd edition, John Wiley & Sons, Inc, 2008
3. Minhang Bao, "Analysis and Design Principles of MEMS Devices",1st edition, Elsevier Science, 2005
4. Stephen Santuria," Microsystems Design", 1st edition, Kluwer Academic Publishers, 2001

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COURSE OUTCOMES

Upon completion of the course, the student will be able to

COs	Statements	K–Level
CO1	Summarize the different processes in fabrication of MEMS	Understand
CO2	Interpret the electrical and mechanical concepts of MEMS	Understand
CO3	Make use of actuation techniques in designing MEMS capacitors	Apply
CO4	Summarize the different circuit and system issues in MEMS	Understand
CO5	Examine the effect of packaging in assembling of microsystems and nano devices	Analyze

COURSE ARTICULATION MATRIX:

POs / COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	-	-	-
CO2	2	1	1	-	-	-
CO3	3	2	3	-	-	1
CO4	2	1	1	-	-	-
CO5	3	3	3	-	-	2
CO	2	2	2	-	-	2
Correlation levels:	1: Slight (Low)		2: Moderate (Medium)			3: Substantial (High)

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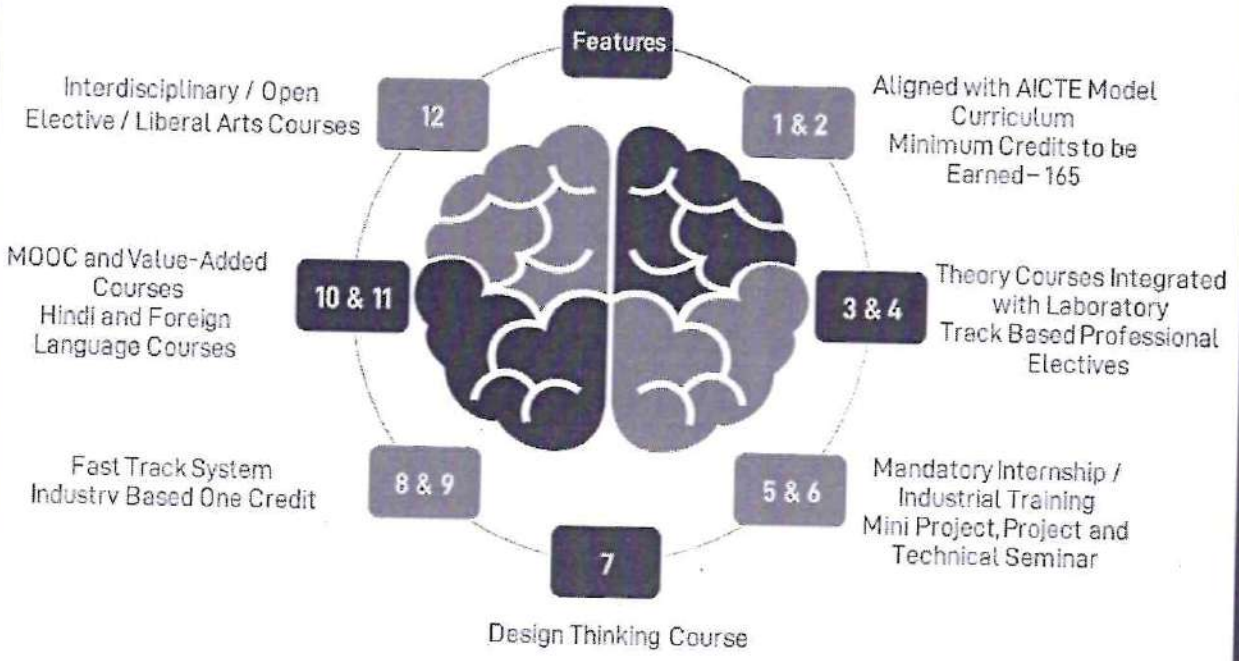
Curriculum Features



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